8. IC 내부 블럭도

8-1 Main

1. AK4355

AK4355

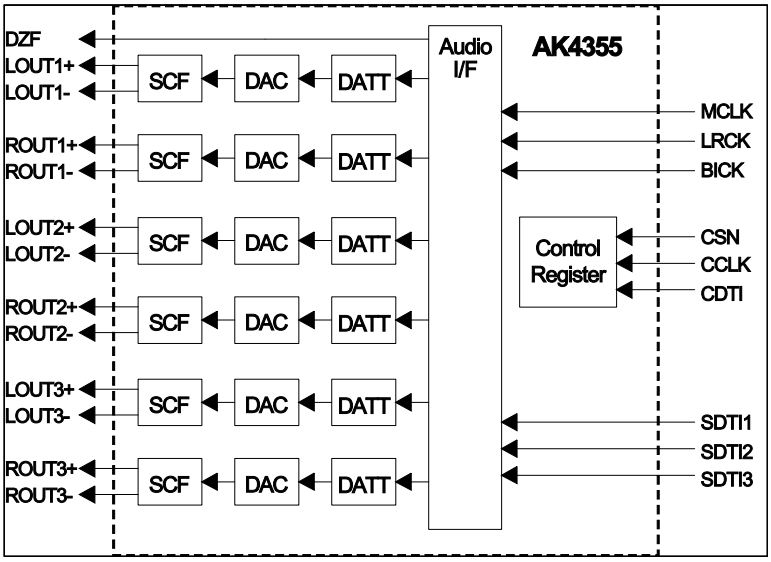
192kHz 24-Bit 6ch DAC for DVD-Audio

GENERAL DESCRIPTION

The AK4355 offers the perfect mix for cost and performance based multi-channel audio systems. AKM's advanced multi-bit architecture delivers a wide dynamic range and low outband noise. The AK4355 has full differential SCF outputs, removing the need for AC coupling capacitors and increasing performance for systems with excessive clock jitter. The 24 Bit word length and 192kHz sampling rate make this part ideal for a wide range of application including DVD-Audio.

FEATURES

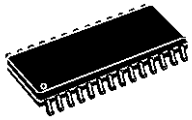
Sampling Rate: 8kHz to 192kHz
24Bit 8 times Digital Filter with Slow roll-off option
THD+N: -90dB
DR, S/N: 106dB
High Tolerance to Clock Jitter
Low Distortion Differential Output
Digital De-emphasis for 32, 44.1 & 48kHz sampling
Zero Detect Pin
Channel Independent Digital Attenuator with soft-transition
Soft Mute
I/F format: 24-Bit MSB justified, 24/20/16-Bit LSB justified or I^2S
Master Clock
Normal Speed: 256fs, 384fs, 512fs or 768fs
Double Speed: 128fs, 192fs, 256fs or 384fs
Quad Speed: 128fs, 192fs
Power Supply: 4.75 to 5.25V
28pin VSOP Package



2. TDA7440D

TONE CONTROL
DIGITALLY CONTROLLED AUDIO PROCESSOR

- INPUT MULTIPLEXER
  - 4 STEREO INPUTS
  - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTATION TO DIFFERENT SOURCES
- ONE STEREO OUTPUT
- TREBLE AND BASS CONTROL IN 2.0dB STEPS
- VOLUME CONTROL IN 1.0dB STEPS
- TWO SPEAKER ATTENUATORS:
  - TWO INDEPENDENT SPEAKER CONTROL IN 1.0dB STEPS FOR BALANCE FACILITY
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTION ARE PROGRAMMABLE VIA SERIAL BUS



SO28

ORDERING NUMBER: TDA7440D

DESCRIPTION

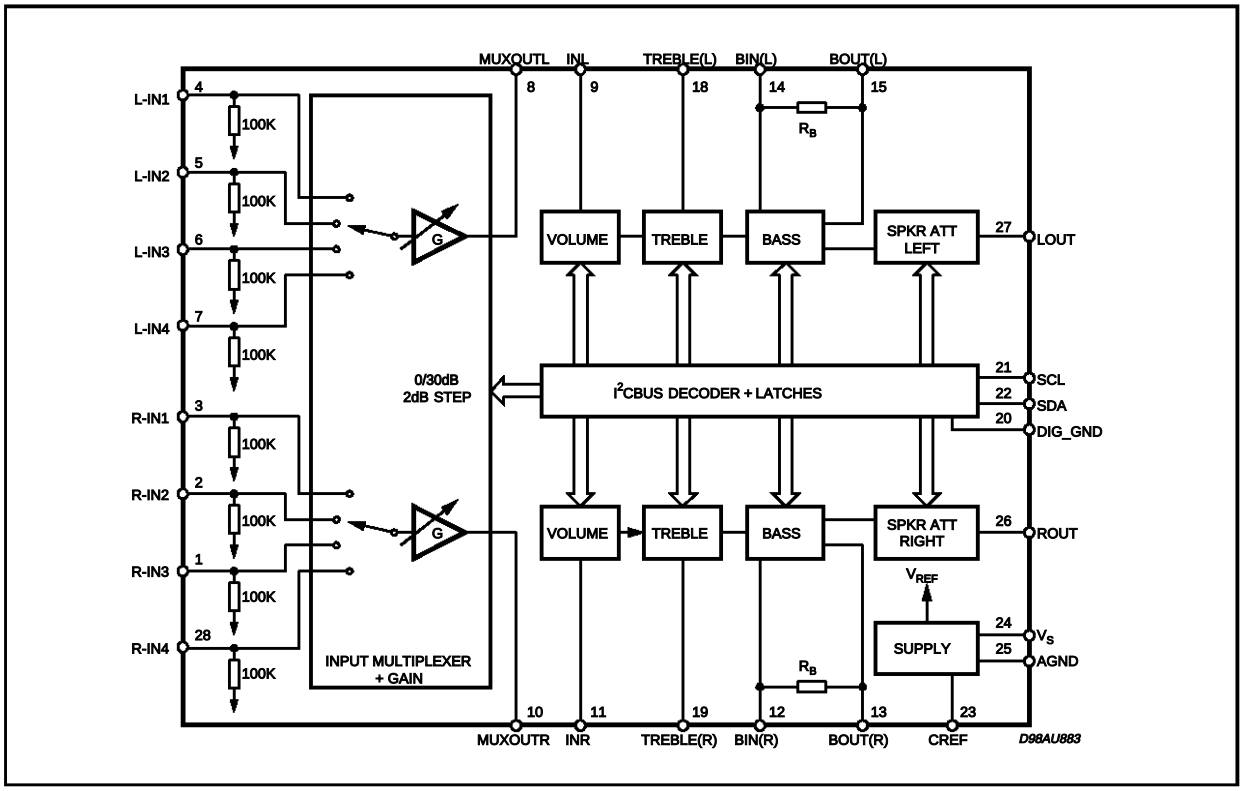
The TDA7440D is a volume tone (bass and treble) balance (Left/Right) processor for quality audio applications in Hi-Fi systems.

Selectable input gain is provided. Control of all the functions is accomplished by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained

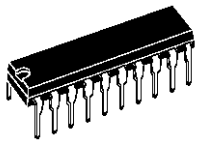
BLOCK DIAGRAM



3. TDA7449L

LOW COST DIGITALLY CONTROLLED AUDIO PROCESSOR

- INPUT MULTIPLEXER
  - 2 STEREO INPUTS
  - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTATION TO DIFFERENT SOURCES
- ONE STEREO OUTPUT
- VOLUME CONTROL IN 1.0dB STEPS
- TWO SPEAKER ATTENUATORS:
  - TWO INDEPENDENT SPEAKER CONTROL IN 1.0dB STEPS FOR BALANCE FACILITY
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTION ARE PROGRAMMABLE VIA SERIAL BUS



DIP20

ORDERING NUMBER: TDA7449L

DESCRIPTION

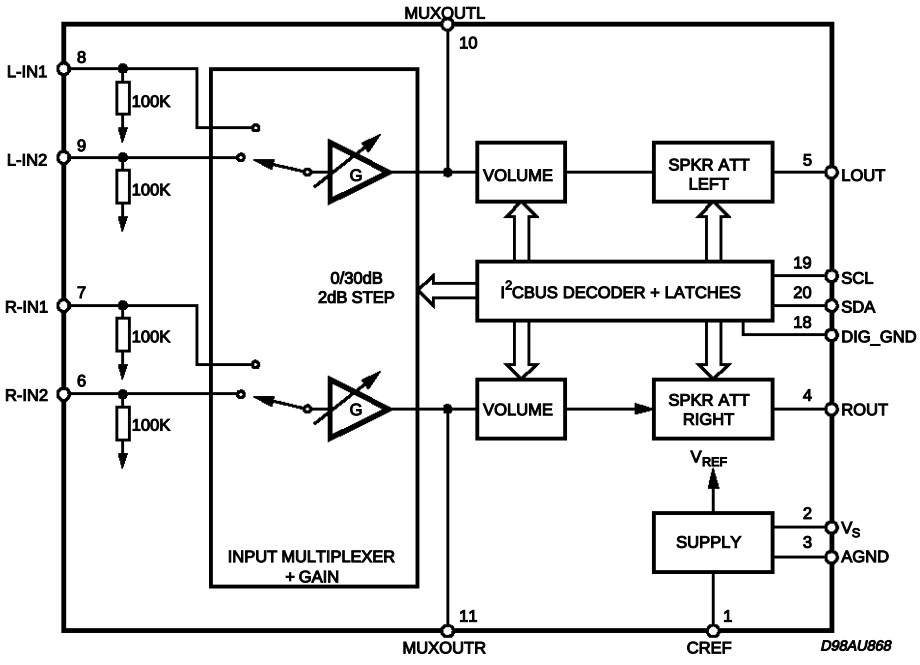
The TDA7449L is a volume control and balance (Left/Right) processor for quality audio applications in TV systems.

Selectable input gain is provided. Control of all the functions is accomplished by serial bus.

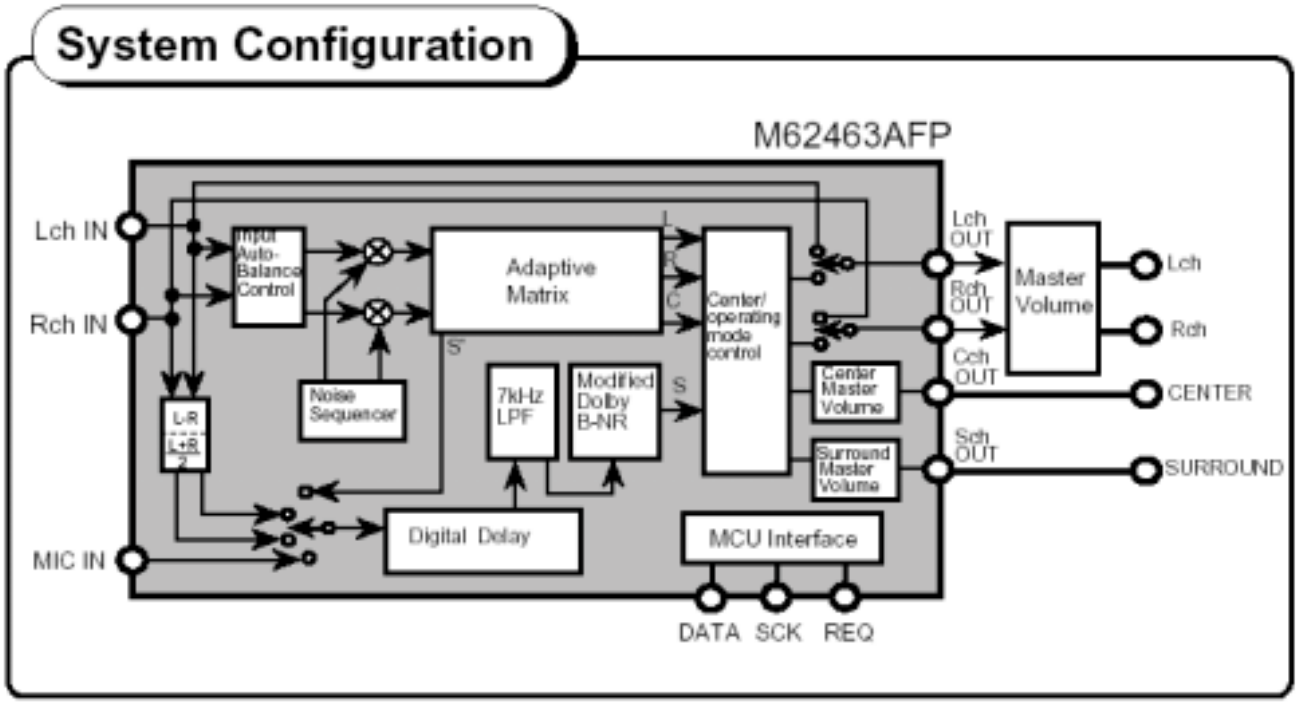
The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

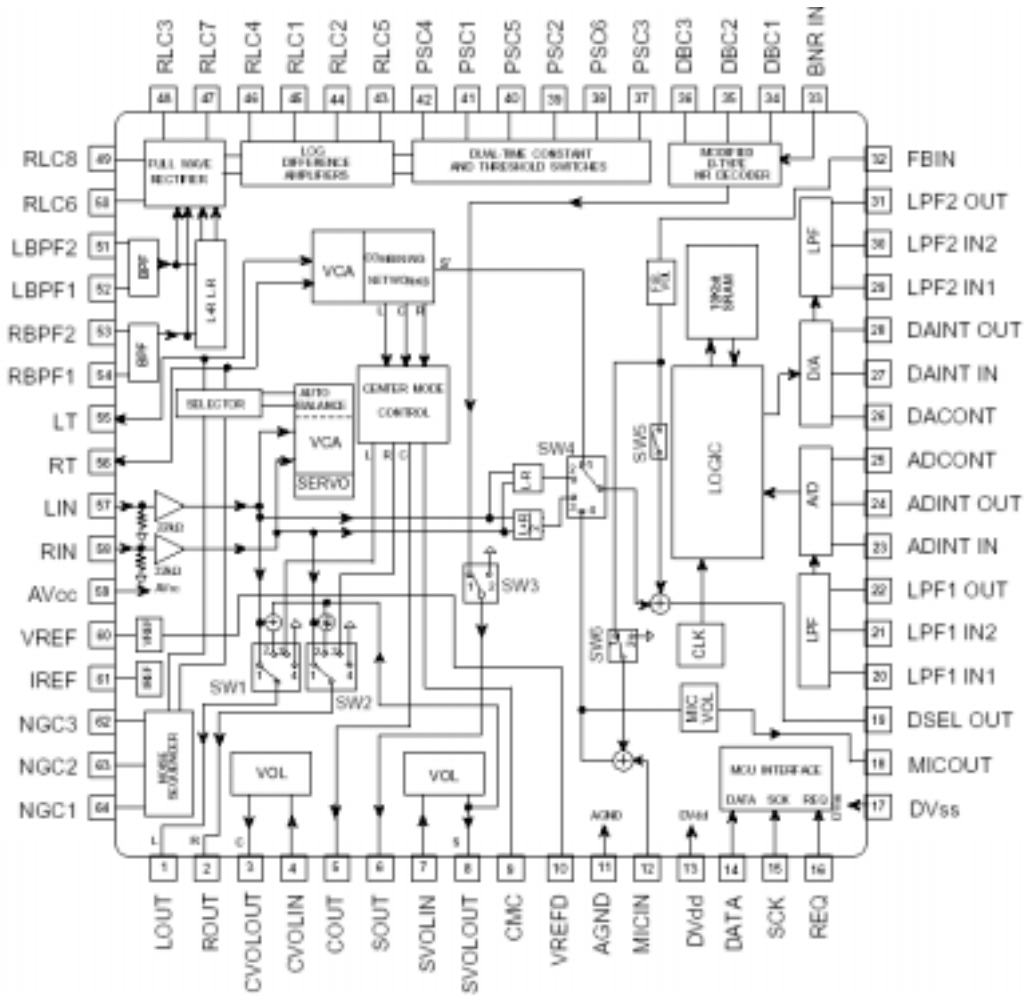
Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained.

BLOCK DIAGRAM

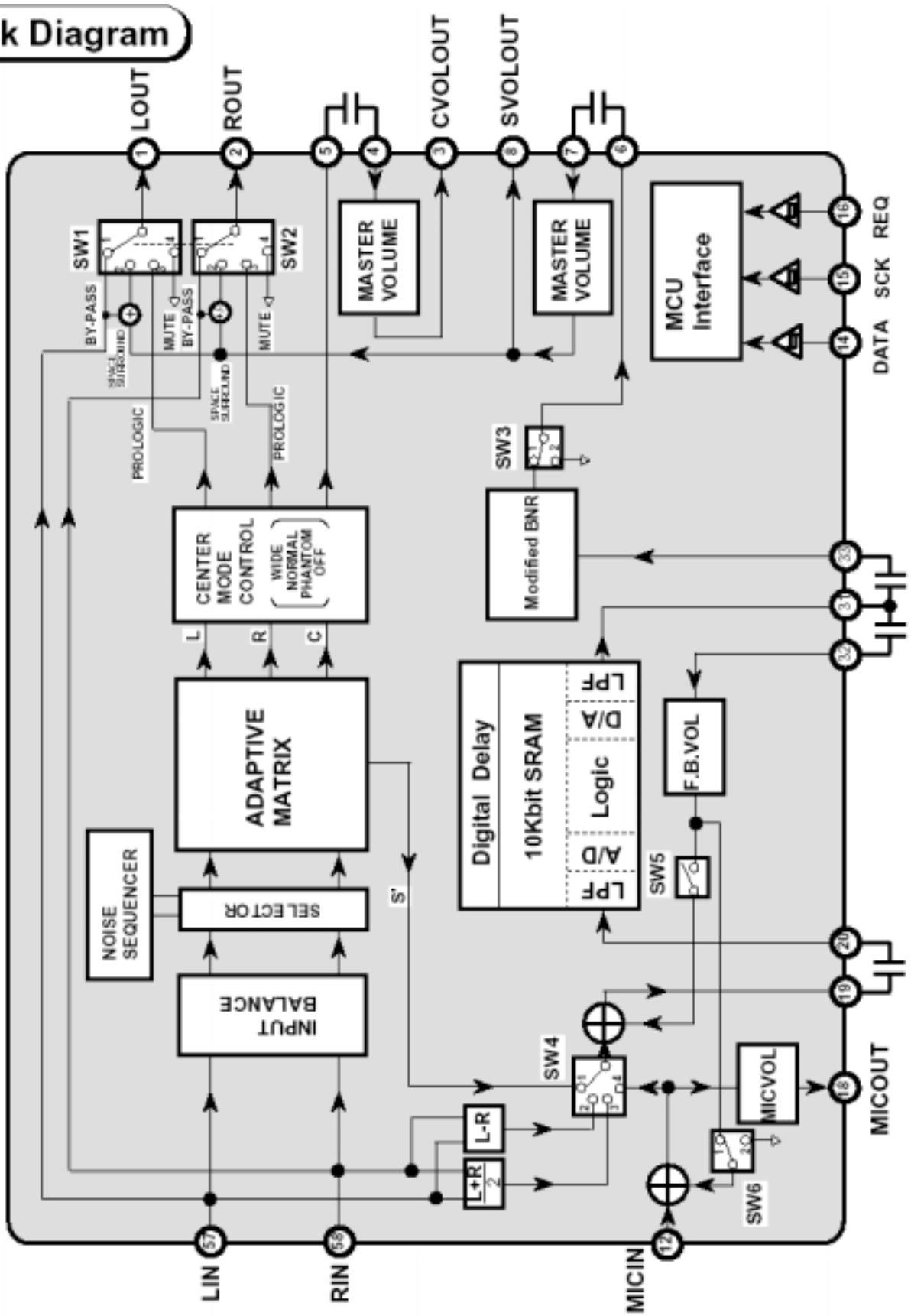


4. M62463AFP


System Configuration
M62463AFP
Lch IN
Rch IN
MIC IN
Input Auto-Balance Control
Noise Sequencer
L-R
L+R
Adaptive Matrix
7kHz LPF
Modified Dolby B-NR
Digital Delay
Center/ operating mode control
Center Master Volume
Surround Master Volume
Master Volume
MCU Interface
Lch OUT
Rch OUT
Cch OUT
Sch OUT
Lch
Rch
CENTER
SURROUND
DATA SCK REQ


RLC3 RLC7 RLC4 RLC1 RLC2 RLC5 PSC4 PSC1 PSC5 PSC2 PSO6 PSC3 DBC3 DBC2 DBC1 BNR IN
RLC8 RLC6 LBPF2 LBPF1 RBPF2 RBPF1 LT RT LIN RIN AVcc VREF IREF NGC3 NGC2 NGC1
FBIN LPF2 OUT LPF2 IN2 LPF2 IN1 DAINT OUT DAINT IN DACONT ADCONT ADINT OUT ADINT IN LPF1 OUT LPF1 IN2 LPF1 IN1 DSEL OUT MICOUT DVss
LOUT ROUT CVOLOUT CVOLIN COUT SOUT SVOLIN SVOLOUT CMC VREFD AGND MICIN DVdd DATA SCK REQ
VCA
SERVO
SELECTOR
CENTER MODE CONTROL
LOGIC
SW1
SW2
SW3
SW4
SW5
SW6
VOL
CLK
MCU INTERFACE

Block Diagram



8-2 DVD

1. ZIVA- 5 DVD CONTROLER

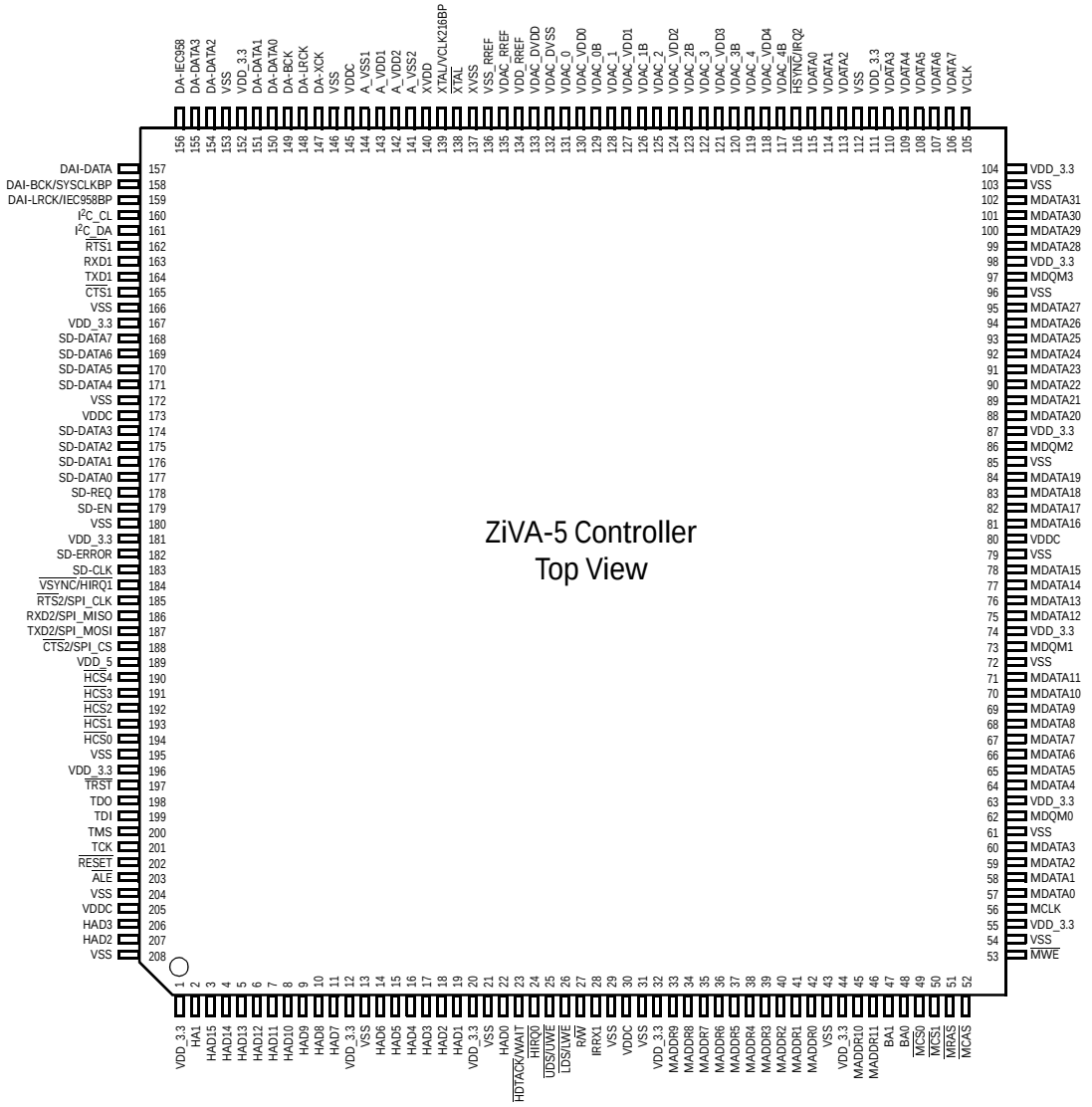


Figure 1 ZiVA-5 controller Pinout (208-pin PQFP)

Table 1 ZiVA-5 controller Pin List

Pin No.	Pin Name	I/O Voltage	I/O Type
1	VDDP	3.3V	ó
2	HA1	3.3V*	I/O
3	HA15	3.3V*	I/O
4	HA14	3.3V*	I/O
5	HA13	3.3V*	I/O
6	HA12	3.3V*	I/O

Table 1 ZiVA-5 controller Pin List (Continued)

Pin No.	Pin Name	I/O Voltage	I/O Type
7	HA11	3.3V*	I/O
8	HA10	3.3V*	I/O
9	HA9	3.3V*	I/O
10	HA8	3.3V*	I/O
11	HA7	3.3V*	I/O
12	VDDP	3.3V	ó
13	GNDP	GROUND	ó
14	HA6	3.3V*	I/O
15	HA5	3.3V*	I/O
16	HA4	3.3V*	I/O
17	HA3	3.3V*	I/O
18	HA2	3.3V*	I/O
19	HA1	3.3V*	I/O
20	VDDP	3.3V	ó
21	GNDP	GROUND	ó
22	HA0	3.3V*	I/O
23	$\overline{\text{HDTACK}}$/WAIT	3.3V*	I/OD
24	$\overline{\text{HIRQ0}}$	3.3V*	I/O
25	$\overline{\text{HUDS}}$/$\overline{\text{UWE}}$	3.3V*	I/O
26	$\overline{\text{HLDS}}$/$\overline{\text{LWE}}$	3.3V*	I/O
27	HREAD	3.3V*	I/O
28	IRRX1/GPIO[0]	3.3V*	I
29	GND	GROUND	ó
30	VDD	1.8V	ó
31	GND25	GROUND	ó
32	VDD25	3.3V	ó
33	MA9	3.3V	O
34	MA8	3.3V	O
35	MA7	3.3V	O
36	MA6	3.3V	O
37	MA5	3.3V	O
38	MA4	3.3V	O
39	MA3	3.3V	O
40	MA2	3.3V	O
41	MA1	3.3V	O
42	MA0	3.3V	O
43	GND25	GROUND	ó
44	VDD25	3.3V	ó
45	MA10	3.3V	O
46	MA11	3.3V	O
47	BA1	3.3V	O
48	BA0	3.3V	O
49	$\overline{\text{MCS0}}$	3.3V	O
50	$\overline{\text{MCS1}}$	3.3V	O
51	$\overline{\text{MRAS}}$	3.3V	O
52	$\overline{\text{MCAS}}$	3.3V	O
53	$\overline{\text{MWE}}$	3.3V	O

Table 1 ZiVA-5 controller Pin List (Continued)

Pin No.	Pin Name	I/O Voltage	I/O Type
54	GND25	GROUND	ó
55	VDD25	3.3V	ó
56	MCLK		O
57	MD0	3.3V	I/O
58	MD1	3.3V	I/O
59	MD2	3.3V	I/O
60	MD3	3.3V	I/O
61	GND25	GROUND	ó
62	MDQM0	3.3V	O
63	VDD25	3.3V	ó
64	MD4	3.3V	I/O
65	MD5	3.3V	I/O
66	MD6	3.3V	I/O
67	MD7	3.3V	I/O
68	MD8	3.3V	I/O
69	MD9	3.3V	I/O
70	MD10	3.3V	I/O
71	MD11	3.3V	I/O
72	GND25	GROUND	ó
73	MDQM1	3.3V	O
74	VDD25	3.3V	ó
75	MD12	3.3V	I/O
76	MD13	3.3V	I/O
77	MD14	3.3V	I/O
78	MD15	3.3V	I/O
79	GND	GROUND	ó
80	VDD	1.8V	ó
81	MD16	3.3V	I/O
82	MD17	3.3V	I/O
83	MD18	3.3V	I/O
84	MD19	3.3V	I/O
85	GND25	GROUND	ó
86	MDQM2	3.3V	O
87	VDD25	3.3V	ó
88	MD20	3.3V	I/O
89	MD21	3.3V	I/O
90	MD22	3.3V	I/O
91	MD23	3.3V	I/O
92	MD24	3.3V	I/O
93	MD25	3.3V	I/O
94	MD26	3.3V	I/O
95	MD27	3.3V	I/O
96	GND25	GROUND	ó
97	MDQM3	3.3V	O
98	VDD25	3.3V	ó
99	MD28	3.3V	I/O
100	MD29	3.3V	I/O

Table 1 ZiVA-5 controller Pin List (Continued)

Pin No.	Pin Name	I/O Voltage	I/O Type
101	MD30	3.3V	I/O
102	MD31	3.3V	I/O
103	GND25	GROUND	ó
104	VDD25	3.3V	ó
105	VCLK	3.3V*	I/O
106	VDATA7/GPIO[1]	3.3V*	I/O
107	VDATA6/GPIO[2]	3.3V*	I/O
108	VDATA5/GPIO[3]	3.3V*	I/O
109	VDATA4/GPIO[4]	3.3V*	I/O
110	VDATA3/GPIO[5]	3.3V*	I/O
111	VDDP	3.3V	ó
112	GNDP	GROUND	ó
113	VDATA2/GPIO[6]	3.3V*	I/O
114	VDATA1/GPIO[7]	3.3V*	I/O
115	VDATA0/GPIO[8]	3.3V*	I/O
116	$\overline{\text{HSYNC}}$/$\overline{\text{HIRQ2}}$/GPIO[9]	3.3V*	I/O
117	VDAC_4B	ANALOG	O
118	VDAC_VDD4	3.3V ANALOG	ó
119	VDAC_4	ANALOG	O
120	VDAC_3B	ANALOG	O
121	VDAC_VDD3	3.3V ANALOG	ó
122	VDAC_3	ANALOG	O
123	VDAC_2B	ANALOG	O
124	VDAC_VDD2	3.3V ANALOG	ó
125	VDAC_2	ANALOG	O
126	VDAC_1B	ANALOG	O
127	VDAC_VDD1	3.3V ANALOG	ó
128	VDAC_1	ANALOG	O
129	VDAC_0B	ANALOG	O
130	VDAC_VDD0	3.3V ANALOG	ó
131	VDAC_0	ANALOG	O
132	VDAC_DVSS	GROUND	
133	VDAC_DVDD 3.	3V	
134	VAC_REFVDD	3.3V	
135	VDAC_REF	ANALOG	I
136	VDAC_REFVSS	GROUND	
137	XVSS	GROUND	
138	XOUT	ANALOG	
139	XIN/bypass clk_216	ANALOG	
140	XVDD	3.3V	
141	AVSS2	GROUND	
142	AVDD2	3.3V	
143	AVDD1	3.3V	
144	AVSS1	GROUND	
145	VDD	1.8V	ó
146	GND	GROUND	ó
147	XCK	3.3V*	I/O

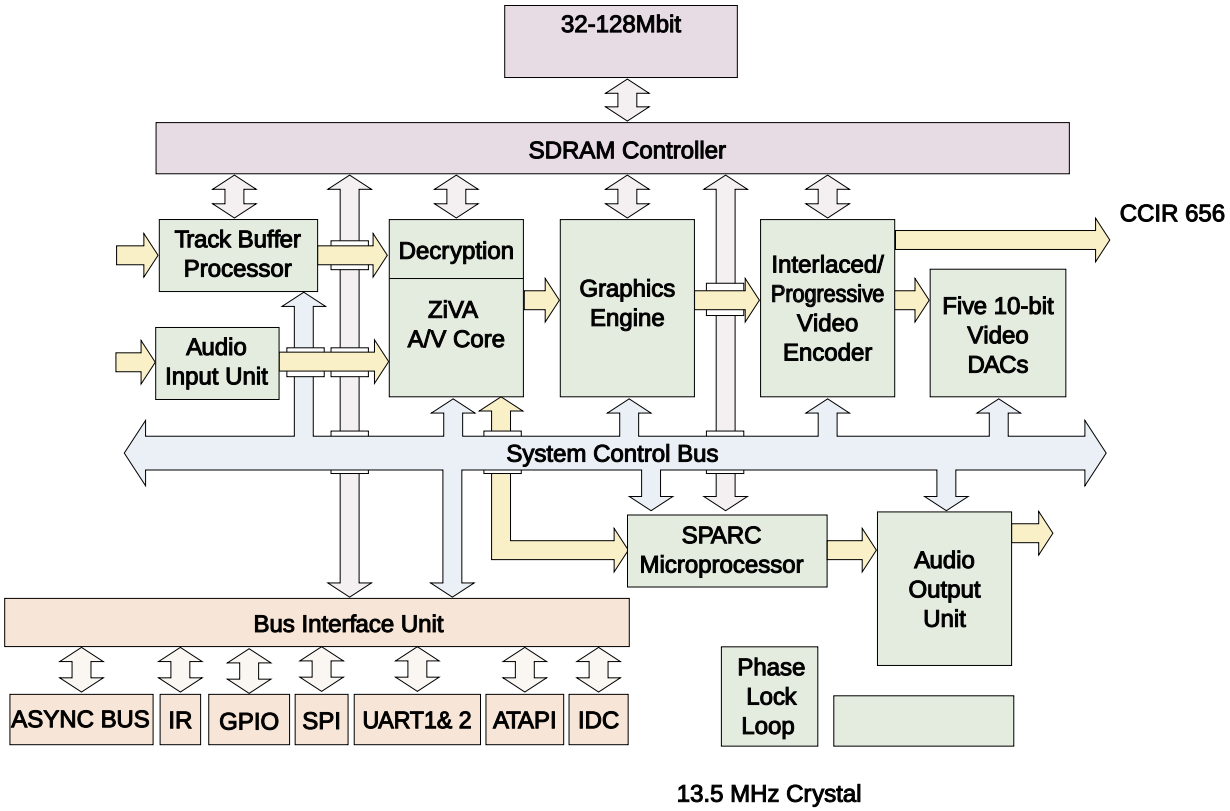
Table 1 ZiVA-5 controller Pin List (Continued)

Pin No.	Pin Name	I/O Voltage	I/O Type
148	LRCK	3.3V*	O
149	BCK	3.3V*	O
150	ADATA0/GPIO[10]	3.3V*	O
151	ADATA1/GPIO[11]	3.3V*	O
152	VDDP	3.3V	ó
153	GNDP	GROUND	ó
154	ADATA2/GPIO[12]	3.3V*	O
155	ADATA3/GPIO[13]	3.3V*	O
156	IEC958/GPIO[14]	3.3V*	O
157	DAI_DATA/GPIO[15]	3.3V*	I
158	DAI_BCK/bypass_sysclk/ GPIO[16]	3.3V*	I
159	DAI_LRCK/iec958bp/GPIO[17]	3.3V*	I
160	I2C_CL/GPIO[18]	3.3V*	I/OD
161	I2C_DA/GPIO[19]	3.3V*	I/OD
162	$\overline{\text{RTS}}$1/GPIO[20]	3.3V*	O
163	RXD1/GPIO[21]	3.3V*	I
164	TXD1/GPIO[22]	3.3V*	O
165	$\overline{\text{CTS}}$1/GPIO[23]	3.3V*	I
166	GNDP	GROUND	ó
167	VDDP	3.3V	ó
168	SDDATA7/VDATA2[7]/ HDMARQ/GPIO[24]	3.3V	I
169	SDDATA6/VDATA2[6]/HXCVR_ EN/ GPIO[25]	3.3V*	I
170	SDDATA5/VDATA2[5]/ HDMACK/GPIO[26]	3.3V*	I
171	SDDATA4/VDATA2[4]/GPIO[27]	3.3V*	I
172	GND	GROUND	ó
173	VDD	1.8V	ó
174	SDDATA3/VDATA2[3]/GPIO[28]	3.3V*	I
175	SDDATA2/VDATA2[2]/GPIO[29]	3.3V*	I
176	SDDATA1/VDATA2[1]/GPIO[30]	3.3V*	I
177	SDDATA0/VDATA2[0] /GPIO[31]	3.3V*	I
178	SDREQ/GPIO[32]	3.3V*	O
179	SDEN/GPIO[33]	3.3V*	I
180	GNDP	GROUND	ó
181	VDDP	3.3V	ó
182	SDERROR/GPIO[34]	3.3V*	I
183	SDCLK/GPIO[35]	3.3V*	I
184	$\overline{\text{VSYNC}}$/$\overline{\text{HIRQ1}}$/GPIO[36]	3.3V*	I/O
185	$\overline{\text{RTS}}$2/SPI_CLK/GPIO[37]	3.3V*	O
186	RXD2/SPI_MISO/GPIO[38]	3.3V*	I
187	TXD2/SPI_MOSI/GPIO[39]	3.3V*	O
188	$\overline{\text{CTS}}$2/SPI_CS/GPIO[40]	3.3V*	I
189	VNW	5V	ó

Table 1 ZiVA-5 controller Pin List (Continued)

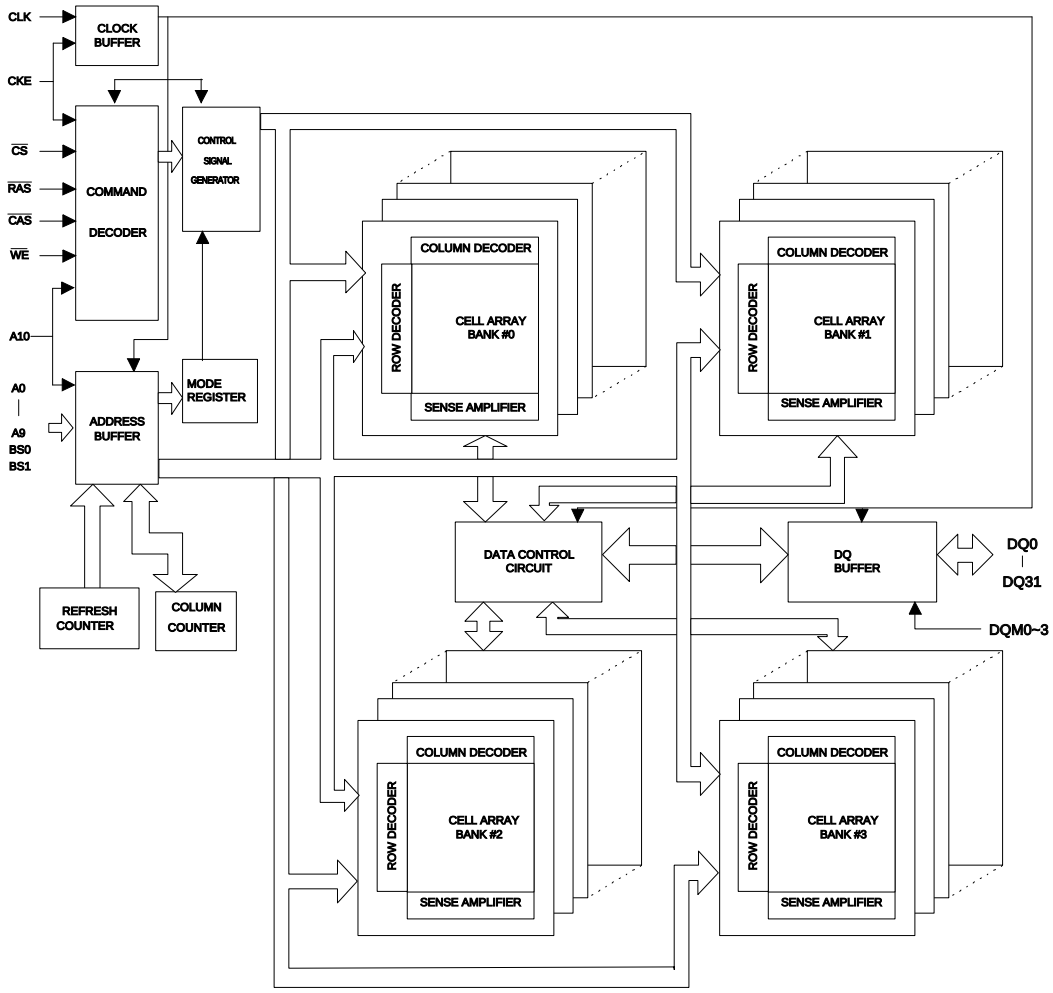
Pin No.	Pin Name	I/O Voltage	I/O Type
190	$\overline{HCS4}$/GPIO[41]	3.3V*	I
191	$\overline{HCS3}$/GPIO[42]	3.3V*	I
192	$\overline{HCS2}$/GPIO[43]	3.3V*	I
193	$\overline{HCS1}$	3.3V*	I/O
194	$\overline{HCS0}$	3.3V*	I/O
195	GNDP	GROUND	ó
196	VDDP	3.3V	ó
197	$\overline{TRST}$	3.3V*	I
198	TDO	3.3V*	O
199	TDI/GPI[0]	3.3V*	I
200	TMS/GPI[1]	3.3V*	I
201	TCK	3.3V*	I
202	$\overline{RESET}$	3.3V*	I
203	$\overline{ALE}$	3.3V*	I/O
204	GND	GROUND	ó
205	VDD	1.8V	ó
206	HA3	3.3V*	I
207	HA2	3.3V*	I
208	GNDP	GROUND	ó

Note: The ZiVA-5 core operates at 1.8V ± 10%. Most I/O interface pins can be interfaced with 3.3-V or 5-V devices depending on the voltage applied to the VDD pins associated with them. Refer to the Application Note for more information.



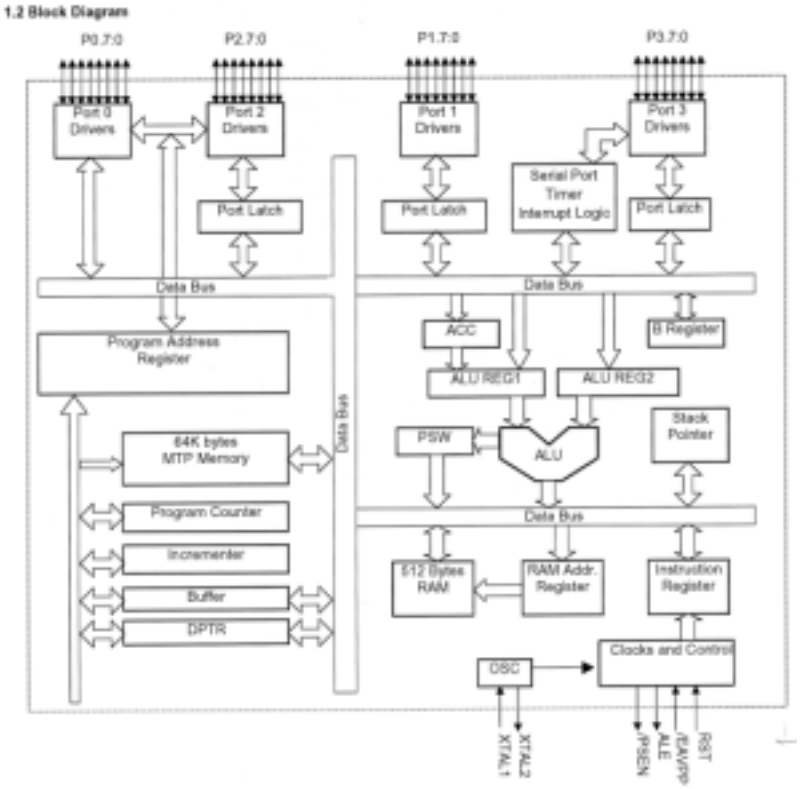
2.W986432DH

BLOCK DIAGRAM

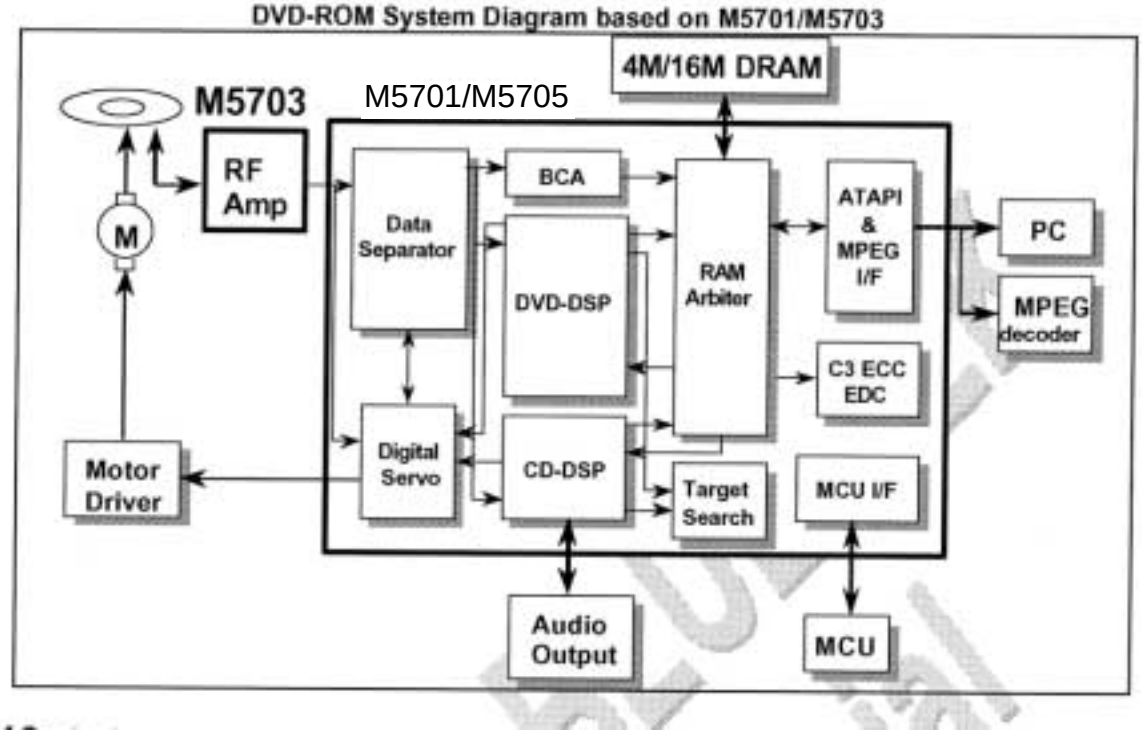


NOTE:
The cell array configuration is 2048 * 256 * 32

3. M6759 ; 8BIT MTP micro controller

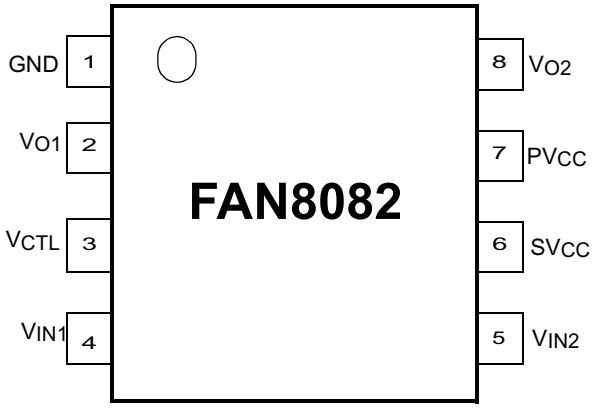


4. M5701/M5705 ; DVD ROM controller



5. FAN8082

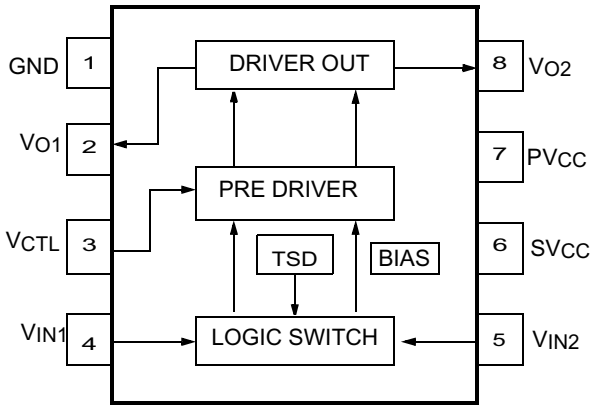
Pin Assignments



Pin Definitions

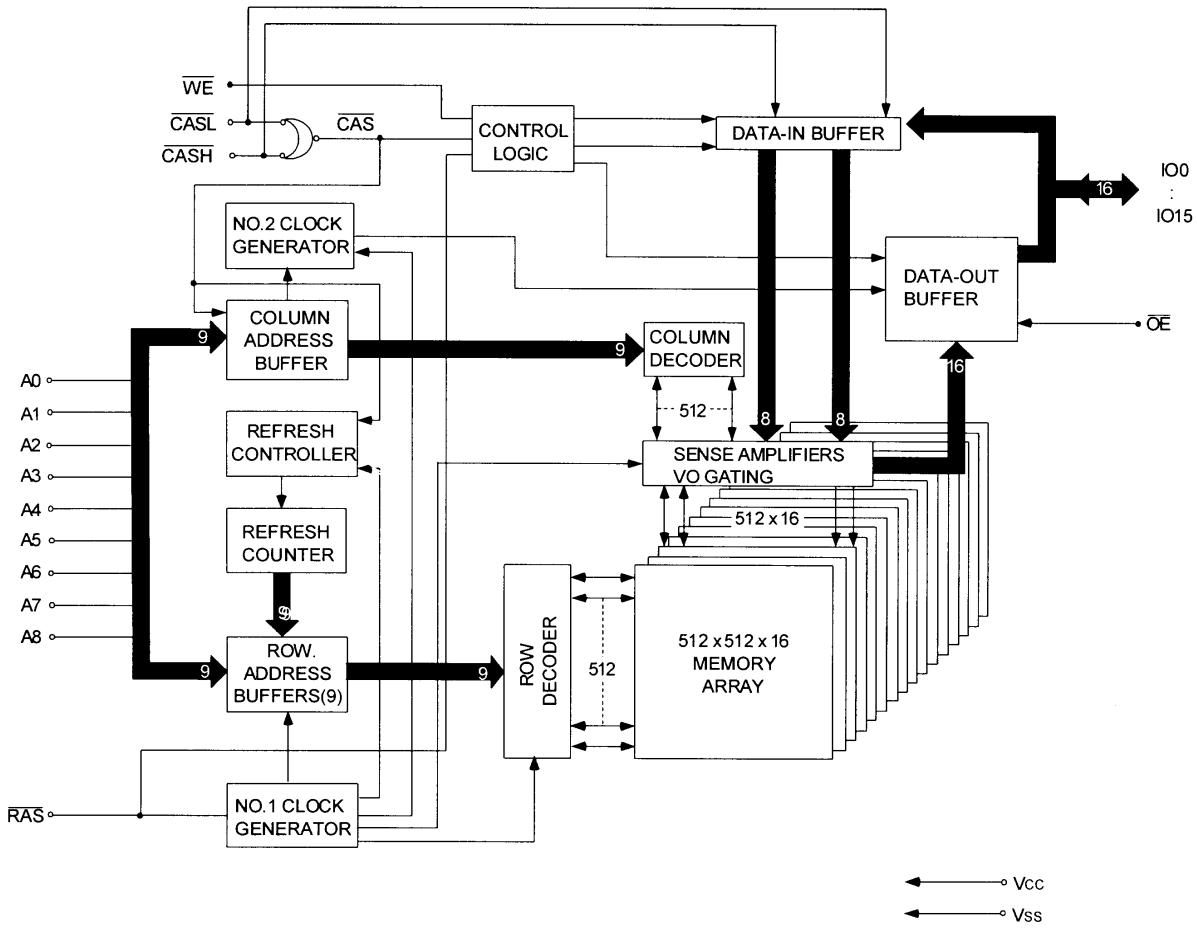
Pin Number	Pin Name	I/O	Pin Function Description
1	GND	-	Ground
2	V_{O1}	O	Output 1
3	V_{CTL}	I	Motor speed control
4	V_{IN1}	I	Input 1
5	V_{IN2}	I	Input 2
6	SV_{CC}	-	Supply voltage (Signal)
7	PV_{CC}	-	Supply voltage (Power)
8	V_{O2}	O	Output 2

Internal Block Diagram



6. M11B416256A

FUNCTIONAL BLOCK DIAGRAM

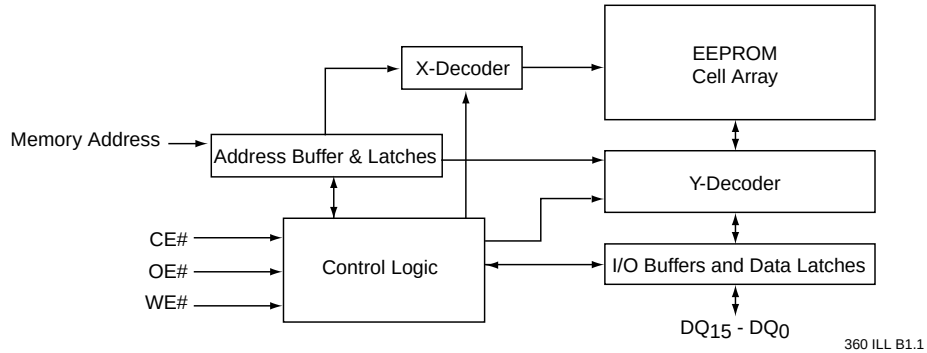


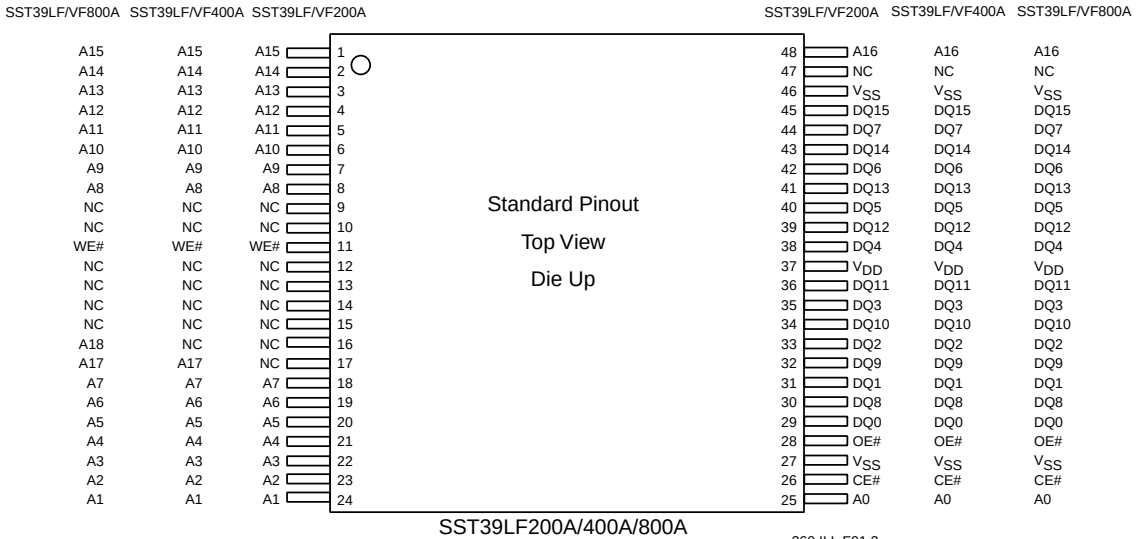
PIN DESCRIPTIONS

PIN NO.	SYM.	TYPE	DESCRIPTION
16~19,22~26	A0~A8	Input	Address Input
14	$\overline{RAS}$	Input	Row Address Strobe
28	$\overline{CASH}$	Input	Column Address Strobe/Upper Byte Control
29	$\overline{CASL}$	Input	Column Address Strobe/Lower Byte Control
13	$\overline{WE}$	Input	Write Enable
27	$\overline{OE}$	Input	Output Enable
2~5,7~10,31~34,36~39	I/O0 ~ I/O15	Input/Output	Data Input/Output
1,6,20	Vcc	Supply	Power, 5V
21,35,40	Vss	Ground	Ground
11,12,15,30	NC	-	No Connect

7. SST39LF800A ; Multi Purpose Flash

FUNCTIONAL BLOCK DIAGRAM





8-3. HT-DM150/550 MICOM PORT ASSIGNMENT

* #31, #47~53 Pull-Down Register (addition)

* GREEN : NC

NO	PORT	NAME	IO	TY	FUNCTION	NO	PORT	NAME	IO	TY	FUNCTION
1	P16/BUZ	RESET	O	CMOS	CS49326/4228/8415 RESET	51	VP	VP	-	-	NC (GND)
2	P17/PWM	P_SCL	O	CMOS	CL-Motor (DVD DOOR)	52	S20/PC4	OPIN5	I	OD	OPTION IN 5 (PULL DOWN)
3	P30	P_SDA	O	CMOS	OP-Motor (DVD DOOR)	53	S21/PC5	OPIN6	I	OD	OPTION IN 6 (PULL DOWN)
4	P31	DO4	O	CMOS	TDA7449 DATA (REAR)	54	S22/PC6	NC	I	OD	NC (PULL DOWN)
5	P32	DO3	O	CMOS	TDA7449 DATA (C/SW)	55	S23/PC7	P_PAVIL	I	OD	Pavilion CNT IN(PULLDOWN)
6	P33	CE1	O	CMOS	LC72131 CE (PLL)	56	S24/PD0	NC	I	OD	NC (PULL DOWN)
7	P34	CS	O	CMOS	CS4228 CS	57	S25/PD1	SW_OP	I	OD	Open(OUT) S/W IN
8	P35	CLK1	O	CMOS	LC72131/TDA7440/7449 CLK	58	S26/PD2	SW_CL	I	OD	Close(IN) S/W IN
9	P36	DO1	O	CMOS	LC72131/TDA7440 DA(FRONT)	59	S27/PD3	M_SEN	I	OD	MIC SENSE (PULL UP)
10	P37	RDSD	I	CMOS	RDS DATA IN	60	S28/PD4	MUTEC	I	OD	CS8228A MUTEC
11	P70/INT0	RDSC	I	OD	RDS CLK IN	61	S29/PD5	U	I	OD	CS8415 U
12	RES	RESET	I	-	MICOM RESET	62	S30/PD6	EMPH	I	OD	CS8415 EMPH
13	P74	XT1	I	-	NC (VDD)	63	S31/PD7	EVR1	I	OD	ELEC VR UP
14	P75	XT2	O	-	NC (OPEN)	64	S32/PE0	EVR2	I	OD	ELEC VR DOWN
15	VSS1	GND	-	-	GND	65	S33/PE1	CDOUT1	I	CMOS	CS49326 SCDOUT
16	CF1	CF1	I	-	MAIN OSC (6MHz) IN	66	S34/PE2	CDOUT2	I	OD	CS8415 CDOUT
17	CF2	CF2	O	-	MAIN OSC (6MHz) OUT	67	S35/PE3	DI1	I	OD	LC72131 DATA IN(PULLDOWN)
18	VDD1	VDD	-	-	VDD	68	S36/PE4	H-SEN	I	OD	HEADPHONE SENSE(PULLDOWN)
19	P80/ANO	NC	I	CMOS	NC (PULL DOWN)	69	S37/PE5	ST	I	OD	STEREO
20	P81/AN1	AD1	I	CMOS	KEY A/D	70	S38/PE6	PROTEC	I	OD	PROTECTION
21	P82/AN2	P-SENS	I	CMOS	POWER SENSE	71	S39/PE7	TUNED	I	OD	TUNED
22	P83/AN3	INT	I	CMOS	CS8415 INT	72	VDD4	VDD	-	-	VFD 5V
23	P84/AN4	A16	O	CMOS	W27L010 A16 (PULL UP)	73	S40/PF0	ML	O	OD	WM8720 ML (PULL DOWN)
24	P85/AN5	A15	O	CMOS	W27L010 A15 (PULL UP)	74	S41/PF1	MC	O	OD	WM8720 MC (PULL DOWN)
25	P86/AN6	OE	O	CMOS	W24L257A SRAM OE (PULL UP)	75	S42/PF2	T-CON	O	OD	DVD POWER ON/OFF(P/D)
26	P87/AN7	MCE	O	CMOS	W27L010 ROM CE (PULL UP)	76	S43/PF3	S-MUTE	O	OD	REAR MUTE (PULL DOWN)
27	P71/INT1	INT	I	CMOS	CS49326 INTREQ	77	S44/PF4	F-MUTE	O	OD	FRONT/SW MUTE (PULL DOWN)
28	P72/INT2	SCE	I	CMOS	DVD REQUEST DVD MICOM	78	S45/PF5	C-MUTE	O	OD	CENTER MUTE (PULL DOWN)
29	P73/INT3	REMO	I	CMOS	REMOCON IN	79	S46/PF6	POWER	O	OD	POWER ON/OFF (PULL DOWN)
30	S0/T0	ECHO1	O	OD	ECHO ON/OFF/VR1(PULL DOWN)	80	S47/PF7	RESTB	O	OD	WM8720 RESETB (PULL DOWN)
31	S1/T1	Pavil	O	OD	Pavilion Output(PULL DOWN)	81	S48/PG0	MD	O	OD	WM8720 MD (PULL DOWN)
32	S2/T2	LED	O	OD	LED ON/OFF (PULL DOWN)	82	S49/PG1	AUTO	O	OD	AUTO BOOT (PULL DOWN)
33	S3/T3	AV1	O	OD	TV SELECTOR 1 (4:3/16:9)	83	S50/PG2	CONTB	O	OD	VIDEO MONITOR SW-B (P/D)
34	S4/T4	GAIN3	O	OD	Gain CNT-DL250(PULL DOWN)	84	S51/PG3	CONTA	O	OD	VIDEO MONITOR SW-A (P/D)
35	S5/T5	GAIN2	O	OD	Gain CNT-DL250(PULL DOWN)	85	PO0	MRST	O	CMOS	DVD RESET
36	S6/T6	GAIN1	O	OD	Gain CNT-DL250(PULL DOWN)	86	PO1	MCE	O	CMOS	DVD REQUEST MAIN MICOM
37	S7/T7	AV2	O	OD	TV SELECTOR 2 (4:3/16:9)	87	PO2	CS3	O	CMOS	CS49326 CS
38	S8/T8	COM_SW	O	OD	COMPONENT OUT SW	88	PO3	CS2	O	CMOS	CS8415 CS
39	S9/T9	H/P_M	O	OD	HEADPHONE MUTE	89	VSS2	VSS	-	-	GND
40	S10/T10	ECHO2	O	OD	ECHO VR (OPEN)	90	VDD2	VDD	-	-	VDD2
41	S11/T11	RELAY	O	OD	SPEAKER RELAY	91	PO4	V-BLK	O	CMOS	VFD DRIVER LC75725 BLK
42	S12/T12	OP 1	O	OD	OPTION OUT 1 / SCART-MUTE	92	PO5	V-DI	O	CMOS	VFD DRIVER LC75725 DI
43	S13/T13	OP 2	O	OD	OPTION OUT 2	93	PO6	V-CE	O	CMOS	VFD DRIVER LC75725 CE
44	S14/T14	OP 3	O	OD	OPTION OUT 3	94	PO7	V-CL	O	CMOS	VFD DRIVER LC75725 CL
45	S15/T15	OP 4	O	OD	OPTION OUT 4	95	P10/S00	RD	O	CMOS	DVD SERIAL DATA OUT
46	VDD3	VDD	-	-	VFD 5V	96	P11/S10	TD	I	CMOS	DVD SERIAL DATA IN
47	S16/PC0	OPIN1	I	OD	OPTION IN 1 (PULL DOWN)	97	P12/SCK0	SCLK	O	CMOS	DVD SERIAL CLK
48	S17/PC1	OPIN2	I	OD	OPTION IN 2 (PULL DOWN)	98	P13/SO1	SCCLK	O	CMOS	CS49326/8415/4228 SCCLK
49	S18/PC2	OPIN3	I	OD	OPTION IN 3 (PULL DOWN)	99	P14/S11	P_CODE	O	CMOS	WIRELESS Data-280 (OPEN)
50	S19/PC3	OPIN4	I	OD	OPTION IN 4 (PULL DOWN)	100	P15/SCK1	CDIN	O	CMOS	CS49326/8415/4228 CDIN